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BUSINESS AND TECHNICIAN EDUCATION COUNCIL

National Certificate in Telecommunications

Sets of model questions and answers for Business and Technician Education Council (BTEC) units are given below. The questions illustrate the types of questions that students may encounter, and are useful as practice material for the skills learned during the course.

Where additional text is given for educational purposes, it is shown within square brackets to distinguish it from information expected of students under examination conditions. Representative time limits for questions are shown, and care has been taken to give model answers that reflect these limits.

We would like to emphasise that the questions are not representative of questions set by any particular college.

BTEC: ELECTRICAL AND ELECTRONIC PRINCIPLES II

The questions in this paper are based on the BTEC's standard unit U81/747. Students are advised to read the notes above

Q1 For the circuit shown in Fig. 1, determine

- the power dissipated in the 8Ω resistor,
- the potential difference, across the 24Ω resistor, and
- the current in each section of the circuit.

(7 min)

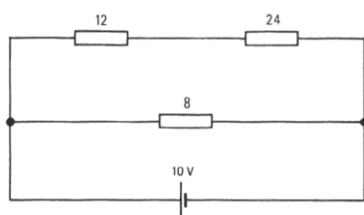


Fig. 1

A1 (a) The power dissipated in the 8Ω resistor

$$= \frac{(\text{voltage})^2}{\text{resistance}} = \frac{100}{8} = 12.5 \text{ W.}$$

- (b) The potential difference across the $12/24\Omega$ resistor circuit is 10 V. Therefore the potential difference across the 24Ω resistor

$$= 10 \times \frac{24}{36} = 6.67 \text{ V.}$$

- (c) The current in the 8Ω resistor

$$= \frac{10}{8} = 1.25 \text{ A.}$$

The current in the $12/24\Omega$ resistor circuit

$$= \frac{10}{36} = 0.28 \text{ A.}$$

The total current flowing from the DC source

$$= 1.25 + 0.28 = 1.53 \text{ A.}$$

Q2 Determine, by Kirchhoff's Laws, the power dissipated in the 6Ω resistor in Fig. 2.

(5 min)

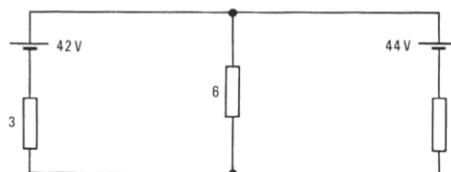
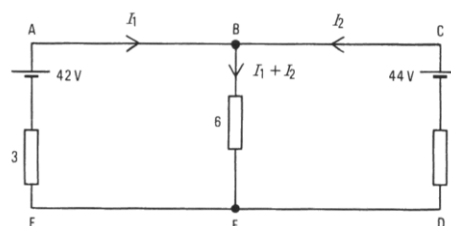


Fig. 2

A2 The sketch shows the assumed current flows.



For circuit ABEF,

$$\begin{aligned} 42 &= 3I_1 + 6(I_1 + I_2), \\ &= 9I_1 + 6I_2. \end{aligned}$$

(1)

For circuit BCDE,

$$\begin{aligned} 44 &= 6(I_1 + I_2) + 2I_2, \\ &= 6I_1 + 8I_2. \end{aligned} \quad (2)$$

Dividing equation (1) by 3 and equation (2) by 4 gives:

$$14 = 3I_1 + 2I_2. \quad (3)$$

$$11 = 1.5I_1 + 2I_2. \quad (4)$$

Subtracting equation (4) from equation (3) gives

$$3 = 1.5I_1.$$

$$\therefore I_1 = 2 \text{ A.}$$

Substituting for I_1 in equation (1),

$$42 = 18 + 6I_2.$$

$$\therefore 6I_2 = 24.$$

$$\therefore I_2 = 4 \text{ A.}$$

The power dissipated in the 6Ω resistor

$$= (I_1 + I_2)^2 \times 6 = 36 \times 6 = \underline{216 \text{ W.}}$$

Q3 For the circuit shown in Fig. 3, determine

- the electric field strength between the x and y plates,
- the charge stored in plate y, and
- the energy stored by the parallel-plate capacitor.

(6 min)

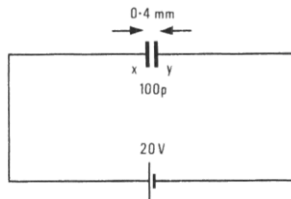


Fig. 3

A3 (a) The electric field strength

$$= \frac{20}{0.4 \times 10^{-3}} \text{ V/m} = \underline{50 \text{ kV/m.}}$$

(b) Let C be the capacitance, and V the voltage.

$$\text{Charge} = CV = 100 \times 10^{-12} \times 20 = \underline{2 \times 10^{-9} \text{ C.}}$$

(c) The energy stored

$$\begin{aligned} &= \frac{1}{2} CV^2, \\ &= \frac{1}{2} \times 100 \times 10^{-12} \times 20 \times 20, \\ &= \underline{0.02 \times 10^{-6} \text{ J.}} \end{aligned}$$

Q4 The cross-sectional area of each plate of an air-dielectric parallel-plate capacitor is 160 cm^2 . If the spacing between the plates is 1.0 mm , determine the capacitance. (The permittivity of free space is $8.85 \times 10^{-12} \text{ F/m}$, and the relative permittivity of air is 1.) (2 min)

A4 The capacitance, C , is given by

$$C = \frac{\epsilon_0 \epsilon_a A}{d},$$

where A is the area in square metres, d is the spacing in metres, ϵ_0 is the permittivity of free space, and ϵ_a is the relative permittivity of air.

$$\begin{aligned} \therefore C &= \frac{8.85 \times 10^{-12} \times 160 \times 10^{-4}}{10^{-3}} \text{ F,} \\ &= \underline{141.6 \text{ pF.}} \end{aligned}$$

Q5 For the circuit shown in Fig. 4, determine

- the total capacitance, and
- the potential difference across the $5 \mu\text{F}$ capacitor.

(4 min)

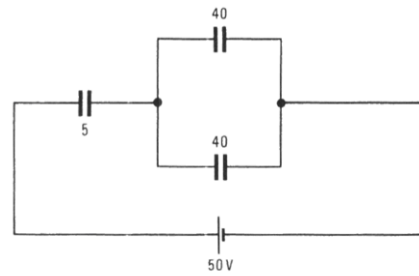


Fig. 4

A5 (a) The capacitance of the parallel circuit

$$= 40 + 40 = 80 \mu\text{F.}$$

Let the total capacitance be C_t .

$$\text{Then, } \frac{1}{C_t} = \frac{1}{5} + \frac{1}{80},$$

$$= \frac{17}{80}.$$

$$\therefore C_t = \frac{80}{17} = \underline{4.7 \mu\text{F.}}$$

(b) The potential difference across the $5 \mu\text{F}$ capacitor

$$= 50 \times \left(\frac{80}{5 + 80} \right) = \underline{47 \text{ V.}}$$

Q6 A capacitor has a charge of $15 \times 10^{-6} \text{ C}$ when 20 V are applied across it; determine the capacitance. (2 min)

A6 The capacitance

$$= \frac{\text{charge}}{\text{voltage}} = \frac{15 \times 10^{-6}}{20} \text{ F} = \underline{0.75 \mu\text{F.}}$$

Q7 Identify points (a), (b) and (c) on the magnetic hysteresis loop shown in Fig. 5. (2 min)

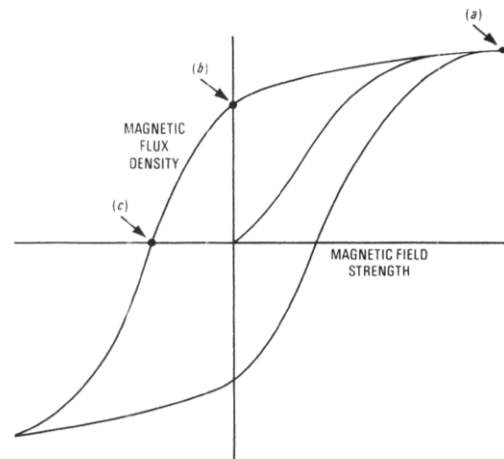


Fig. 5

A7 (a) is the saturation region of the magnetic material.

(b) is the value of magnetic intensity remaining when the magnetising force has been reduced from a maximum to zero, and is known as the remanence.

(c) is the value of the magnetising force required to reduce the magnetic intensity from the remanence value to zero, and is known as the coercive force.

Q8 Determine the magnetic field strength and MMF required to produce a flux density of 0.1 T in an air gap of 0.5 mm . (Permeability of free space $= 4\pi \times 10^{-7} \text{ H/m}$, and the relative permeability of air $= 1$.) (3 min)

A8 The magnetic field strength, H , is given by

$$H = \frac{B}{\mu_0 \mu_{\text{air}}},$$

where B is the flux density, μ_0 is the permeability of free space, and μ_{air} is the relative permeability of air.

$$\therefore H = \frac{0.1}{4\pi \times 10^{-7} \times 1} = 79\,577 \text{ A/m.}$$

If l is the length of the air gap,

$$\begin{aligned} \text{MMF} &= Hl = 79\,577 \times 0.5 \times 10^{-3}, \\ &= \underline{39.79 \text{ A.}} \end{aligned}$$

Q9 The mean diameter of a toroidally wound 1500 turn coil is 5 cm . Determine the MMF when the coil carries 1 A . (2 min)

A9 If N is the number of turns, and I is the current, then

$$\text{MMF} = NI = 1500 \times 1 = \underline{1500 \text{ A.}}$$

Q10 The inductance of a coil is 2 mH when it is carrying a current of 5 A . If the flux produced is $10 \mu\text{Wb}$, determine the number of turns in the coil. (2 min)

A10 Let L be the inductance of the coil, I the current, and Φ the flux. The number of turns is given by

$$\frac{LI}{\Phi} = \frac{2 \times 10^{-3} \times 5}{10 \times 10^{-6}} = \underline{1000 \text{ turns.}}$$

Q11 A transformer reduces its applied voltage by 50% . If the primary winding has 300 turns, determine the number of turns in the secondary. (2 min)

A11 The step-down ratio of the transformer $= 2:1$.

If N_{py} , N_{sy} are the numbers of turns on the primary and secondary windings, respectively, then

$$\frac{N_{\text{py}}}{N_{\text{sy}}} = \frac{2}{1}.$$

$$N_{\text{sy}} = \frac{N_{\text{py}}}{2} = \frac{300}{2} = \underline{150 \text{ turns.}}$$

Q12 A coil has an inductance of 80 mH and carries a current of 45 mA . Determine the energy stored in the coil. (2 min)

A12 Let L be the inductance and I be the current.

$$\begin{aligned} \text{Energy stored} &= \frac{1}{2} LI^2, \\ &= \frac{1}{2} \times 80 \times 10^{-3} \times 45 \times 45 \times 10^{-6} \text{ J}, \\ &= \underline{81 \mu\text{J.}} \end{aligned}$$

Q13 A magnetic flux of 2 mWb links with a coil of 200 turns. If the flux rises uniformly to 5 mWb in 4 ms , determine the value of the induced EMF. (2 min)

A13 The induced EMF $= N \frac{\delta\Phi}{\delta t}$,

where $\delta\Phi$ = change in flux $= 3 \text{ mWb}$,
 δt = time for change $= 4 \text{ ms}$, and
 N = number of turns.

$$\text{Thus, EMF} = 200 \times \frac{3}{4} = \underline{150 \text{ V.}}$$

Q14 A magnetic circuit has a coil of inductance 25 mH and 500 turns. Determine the reluctance of the circuit. (2 min)

A14 Let N be the number of turns, and L the inductance.

$$\text{Reluctance} = \frac{N^2}{L} = \frac{500 \times 500}{25 \times 10^{-3}} = \underline{10^7 \text{ A/Wb.}}$$

Q15 A coil of an electrical instrument has a radius of 1.2 cm and an overall length of 2.5 cm . If the 120 turns of the coil carries 2 A when placed in a flux density of 0.4 T , determine the maximum torque developed. (3 min)

A15 The maximum torque, T_{max} , is given by

$$T_{\text{max}} = 2NBILr,$$

where N is the number of turns,

B is the flux density,

I is the current,

L is the length of the coil, and

r is the radius.

$$\begin{aligned} \therefore T_{\text{max}} &= 2 \times 120 \times 0.4 \times 2 \times 2.5 \times 1.2 \times 10^{-4}, \\ &= \underline{0.0576 \text{ N m.}} \end{aligned}$$

Q16 For the signal shown in Fig. 6, determine

- the repetition frequency,
- the average value of the wave, and
- the RMS value of the wave.

(8 min)

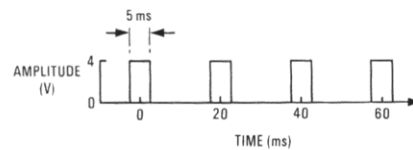


Fig. 6

A16 (a) Repetition frequency

$$= \frac{1}{\text{period}} = \frac{1}{20 \times 10^{-3}} = \underline{50 \text{ Hz.}}$$

$$(b) \text{ Average value} = \frac{5 \times 4}{20} = \underline{1 \text{ V.}}$$

$$(c) \text{ RMS value} = \sqrt{\left(\frac{5 \times 4^2}{20}\right)} = \underline{2 \text{ V.}}$$

Q17 A sinusoidal EMF, expressed by $v = 2.5 \sin 942t$, is connected across a load of 200Ω . Determine

- the frequency of the voltage,
- the value of the current in the load 5 ms after the start of a cycle, and
- the average power dissipated in the load.

(6 min)

$$\text{A17 (a) Frequency} = \frac{942}{2\pi} = \underline{150 \text{ Hz.}}$$

(b) Current after 5 ms

$$\begin{aligned} &= \frac{2.5 \sin(942 \times 5 \times 10^{-3})}{200}, \\ &= 12.5 \sin 4.71 \text{ mA}, \\ &= 12.5 \sin 270^\circ \text{ mA}, \\ &= \underline{-12.5 \text{ mA.}} \end{aligned}$$

$$(c) \text{ Average power} = \frac{1}{2} \times (\text{maximum voltage}) \times (\text{maximum current}),$$

$$\begin{aligned} &= \frac{1}{2} \times 2.5 \times 12.5, \\ &= \underline{15.625 \text{ mW.}} \end{aligned}$$

Q18 Sketch the output waveform (v_o) of the circuit shown in Fig. 7 for the input waveform (v_i) given. (1 min)

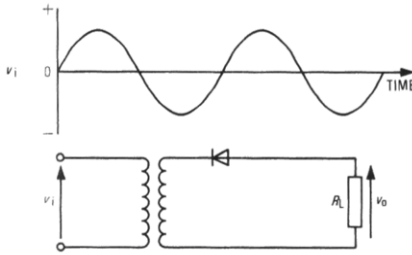
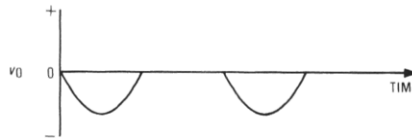


Fig. 7

A18



Q19 A sinusoidal voltage is applied to a resistor of 20Ω . If the RMS voltage is 10.6 V , determine

- the peak voltage, and
- the average voltage.

A19 (a) Peak voltage = $\frac{\text{RMS voltage}}{0.707} = \frac{10.6}{0.707} = 15\text{ V}$. (4 min)

(b) Average voltage = $15 \times 0.637 = 9.56\text{ V}$.

Q20 An AC current of 2 mA at 3000 Hz flows in a series RL circuit. If $R = 2000\Omega$ and $L = 150\text{ mH}$, determine

- the reactance of L , and
- the supply voltage by a phasor diagram.

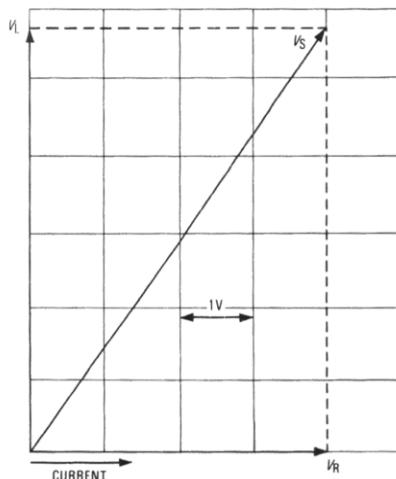
(6 min)

A20 (a) Let f be the frequency and X_L the reactance.

$$\text{Then, } X_L = 2\pi fL = 2\pi \times 3000 \times 150 \times 10^{-3}, \\ = 2827\Omega.$$

(b) The voltage across the inductor, V_L ,
 $= 2827 \times 2 \times 10^{-3} = 5.654\text{ V}.$

The voltage across the resistor, V_R ,
 $= 2000 \times 2 \times 10^{-3} = 4\text{ V}.$



Thus, from the phasor diagram the supply voltage $V_s = 6.9\text{ V}$.

Q21 An AC voltage is applied to a series LCR circuit. What condition will allow maximum current to flow? ($\frac{1}{2}$ min)

A21 When the reactance of the inductor equals the reactance of the capacitor.

Q22 In a series RC circuit, the reactance of the capacitor is 240Ω at 7000 Hz . Determine

- the value of the capacitor, and
- the impedance of the circuit if the resistor value is 100Ω . (4 min)

A22 (a) Let the frequency be f and the reactance of the capacitor be X_c .

$$\text{Then, } X_c = \frac{1}{2\pi fC}. \\ \therefore C = \frac{1}{2\pi fX_c}, \\ = \frac{1}{2\pi \times 7000 \times 240}\text{ F}, \\ = 0.095\mu\text{F}.$$

(b) The impedance of the circuit

$$= \sqrt{R^2 + X_c^2} = \sqrt{(10000 + 57600)} = 260\Omega.$$

Q23 In a series LR circuit, the inductor has a reactance of 70Ω and the resistor a resistance of 50Ω . Determine the phase angle between the supply voltage and current. (2 min)

A23 Let R be the resistance, X_L be the reactance of the inductor and θ be the phase angle.

$$\text{Then, } \tan \theta = \frac{X_L}{R} = \frac{70}{50} = 1.4. \\ \therefore \theta = 54.5^\circ.$$

Q24 In a series LCR circuit, $L = 20\text{ mH}$, $C = 2\mu\text{F}$ and $R = 10\Omega$. Determine the resonant frequency and hence the magnification factor. (5 min)

A24 Let f be the frequency.

Then, at resonance,

$$2\pi fL = \frac{1}{2\pi fC}. \\ \therefore f = \frac{1}{2\pi\sqrt{LC}} = \frac{1}{2\pi\sqrt{(20 \times 10^{-3} \times 2 \times 10^{-6})}}, \\ = 796\text{ Hz}.$$

The magnification factor

$$= \frac{2\pi fL}{R} = \frac{2\pi \times 796 \times 20 \times 10^{-3}}{10} = 10.$$

Q25 The true power of an AC circuit is given as 300 mW . If the power factor is 0.4 , determine the apparent power. (2 min)

$$\text{A25 Power factor} = \frac{\text{true power}}{\text{apparent power}}.$$

$$\text{Thus, apparent power} = \frac{300}{0.4} = 750\text{ mW}.$$

Q26 Explain why the resistance of a semiconductor falls with increase in temperature. (3 min)

A26 As the temperature of a semiconductor rises, hole/electron pairs are generated. The released electrons become available as current carriers, thereby increasing the number of 'free' electrons. The more free electrons in a conducting material, the lower its resistance becomes.

Q27 Draw to scale the impedance triangle for the circuit conditions shown in Fig. 8. (6 min)

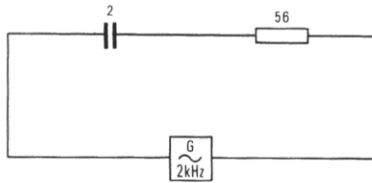


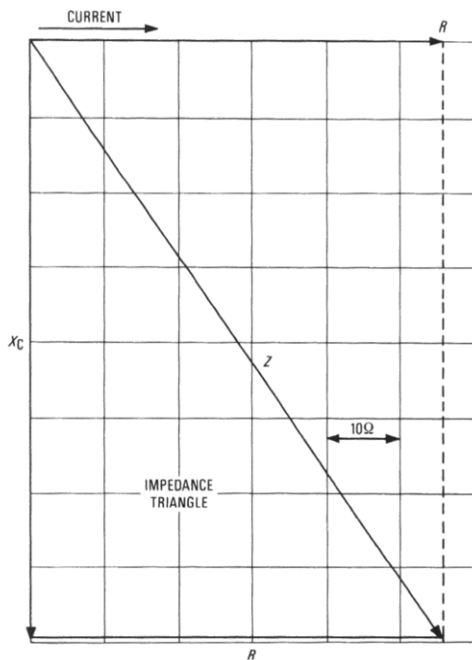
Fig. 8

A27 Let X_C be the impedance of the capacitor, R the resistance, f the frequency, and C the capacitance.

$$\text{Then, } X_C = \frac{1}{2\pi fC} = \frac{1}{2\pi \times 2000 \times 2 \times 10^{-6}},$$

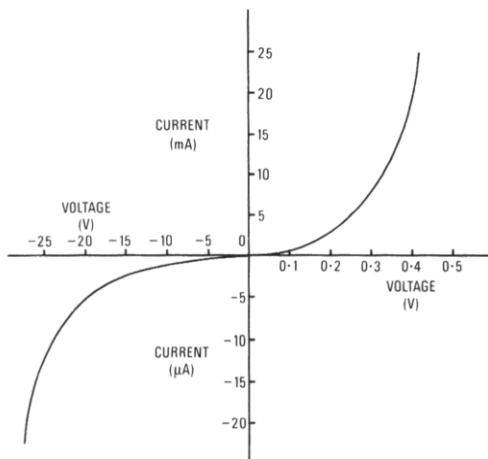
$$= 79.57 \Omega.$$

The impedance triangle is shown in the sketch. Z is the total impedance, $R = 56 \Omega$.



Q28 Sketch a typical forward/reverse bias characteristic of a p-n junction. (2 min)

A28

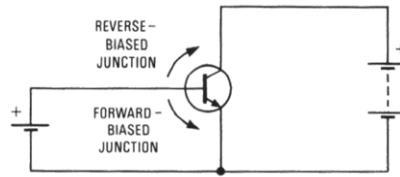


Q29 What current carrier provides the current in a reverse-biased p-n junction? (½ min)

A29 The minority current carrier.

Q30 Sketch a transistor connected in common-emitter mode, and indicate the bias voltage condition of the junctions. (2 min)

A30

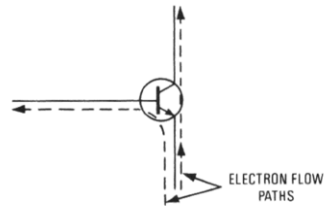


Q31 Is a transistor a current- or voltage-operated device? (½ min)

A31 Current-operated device.

Q32 On the circuit symbol of an n-p-n transistor, show the electron flow paths of the transistor. (2 min)

A32

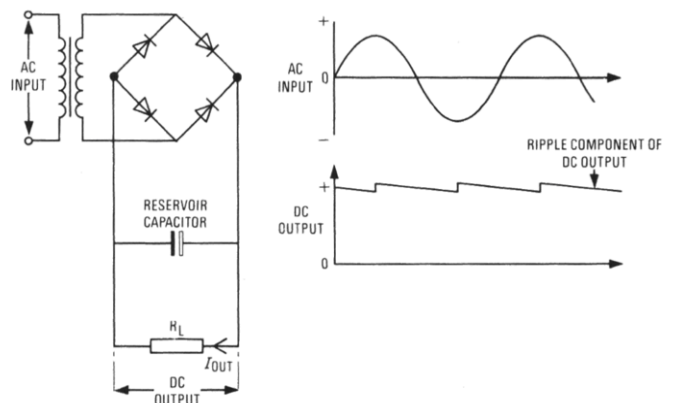


Q33 Name the common semiconductor materials used in diode and transistor components. (½ min)

A33 Germanium and silicon.

Q34 Draw the circuit diagram of a full-wave bridge rectifier. Show on your diagram the AC input, the DC output and the direction of the current flow through the load resistance. (6 min)

A34



Q35 A moving-coil meter has a full-scale deflection when a current of 15 mA flows through it. The resistance of the meter is 4 Ω. Determine the shunt resistance needed for the meter to have a measurement range of 0–50 A. Draw the circuit diagram of the modified meter. (4 min)

A35 Maximum current to be measured = 50 A.

Maximum current required to pass through the meter coil to give full-scale deflection = 15 mA.

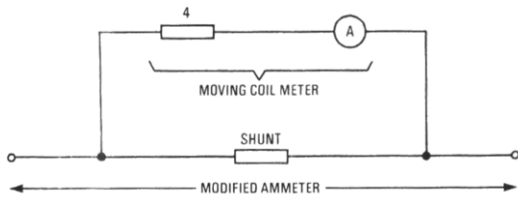
Thus current to be diverted = $50 - 0.015 = 49.985$ A.

At full-scale deflection the potential difference across the meter = $4 \times 0.015 = 0.06$ V. This voltage will also be across the shunt.

Therefore, shunt resistance

$$= \frac{0.06}{49.985} = 0.0012 \Omega.$$

The circuit of the modified meter is shown in the sketch.



Q36 For the transistor characteristics shown in Fig. 9, determine the current gain of the transistor at $V_{CE} = 5$ V. State all reference points. (V_{CE} is the collector-emitter voltage, I_C is the collector current, and I_B is the base current). (5 min)

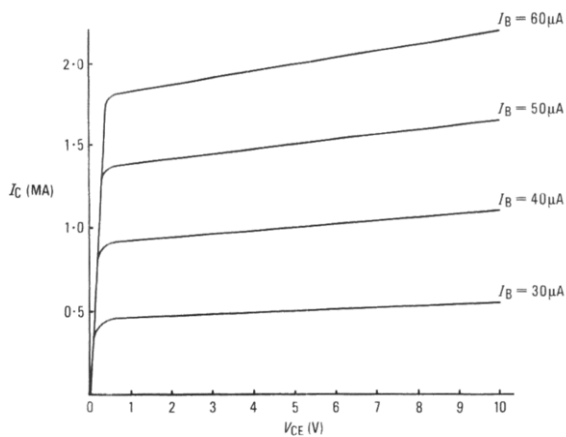
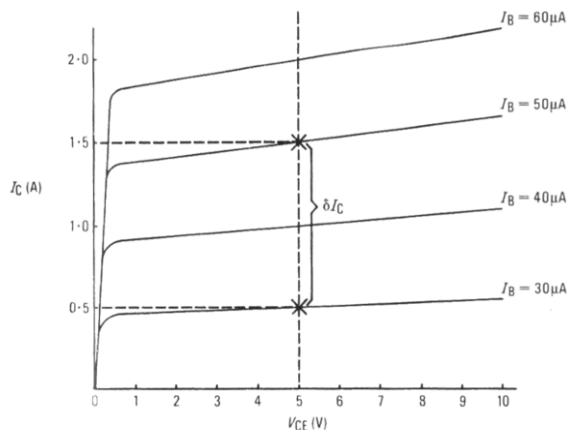


Fig. 9

A36



See sketch. Corresponding I_C values are taken for I_B values at the intersection of the $V_{CE} = 5$ V reference line. In this case, I_B values of $30 \mu\text{A}$ and $50 \mu\text{A}$ have been used for the calculation. The corresponding values of I_C are 0.5 mA and 1.5 mA, respectively.

The current gain at $V_{CE} = 5$ V is given by $\delta I_C / \delta I_B$, where δI_C is a small change in I_C , and δI_B is a small change in I_B .

Thus current gain

$$= \frac{(1.5 - 0.5) \times 10^{-3}}{(50 - 30) \times 10^{-6}} = \frac{1}{20} \times 10^3 = 50.$$

Q37 Determine the resistance of a voltmeter on a voltage range of $0-100$ V. The sensitivity of the instrument is $20000 \Omega/\text{V}$. (2 min)

A37 Meter resistance

$$\begin{aligned} &= \text{sensitivity} \times \text{maximum value of the range,} \\ &= 20000 \times 100, \\ &= \underline{2 \text{ M}\Omega}. \end{aligned}$$

Q38 What instrument is capable of measuring time and voltage simultaneously? ($\frac{1}{2}$ min)

A38 The cathode-ray oscilloscope.

Q39 Fig. 10 shows the circuit conditions of a Wheatstone bridge at balance. Determine the value of R_x . (2 min)

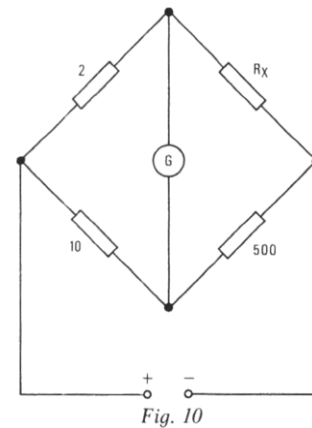


Fig. 10

A39

$$\frac{R_x}{500} = \frac{2}{10}.$$

$$\therefore R_x = \frac{2 \times 500}{10} = \underline{100 \Omega}.$$

Q40 What is the ideal design requirement for

- an ammeter, and
- a voltmeter?

(2 min)

A40 (a) Ideally, an ammeter should have zero resistance so that a true current reading of the circuit being tested can be obtained.

(b) Ideally, a voltmeter should have infinite impedance to avoid disturbing the circuit being tested.

Q41 What is the major advantage of digital measuring instruments over analogue instruments in terms of operator usage? (3 min)

A41 Analogue instruments use a pointer to indicate the value of a reading. The scale can be misread unless the eye of the operator is directly over the pointer. This means that the meter must always be conveniently placed near to the operator. Digital instruments give a direct numerical readout thus avoiding operator readout errors. Also, as the instrument gives a numerical display, it can be positioned anywhere within reasonable viewing range of the operator.

Questions and answers contributed by N. C. Webber

The questions in this paper are based on the BTEC's standard unit U81/751. Students are advised to read the notes on p. 29

Q1 Complete the table given below, which shows a comparison between transistor-transistor logic (TTL), emitter-coupled logic (ECL) and complementary metal-oxide semiconductor (CMOS) logic gates.

	TTL	ECL	CMOS
Power Supply Voltage			
Fan-Out			
Propagation Delay			

(4 min)

A1

	TTL	ECL	CMOS
Power Supply Voltage	+5 V	-5.2 V	3-18 V
Fan-Out	10	100+	50
Propagation Delay	20 ns	3 ns	50 ns

Q2 Identify the circuit shown in Fig. 1 and briefly describe its operation. (6 min)

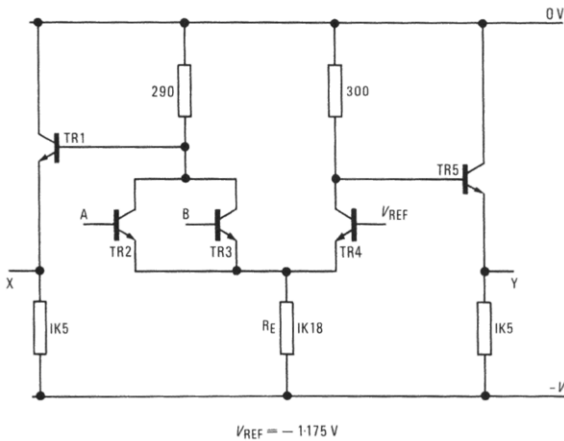


Fig. 1

A2 The circuit shown is an emitter-coupled logic (ECL) OR/NOR gate.

The ECL gate works by diverting the almost constant current which flows through resistor R_E into either transistor TR2, transistor TR3, transistors TR2 and TR3, or transistor TR4.

If the voltages at inputs A and B are below the reference voltage V_{REF} , then both transistors TR2 and TR3 are OFF. Their common collector voltage is HIGH and thus the output voltage X is also HIGH. This corresponds to logic state 0 at both inputs, and logic state 1 at the output. Transistor TR4 is conducting current and, therefore, its collector voltage is LOW.

If one or both of the inputs are now connected to an input voltage which is higher than the reference voltage V_{REF} , current is diverted away from transistor TR4, which turns OFF. The collector voltage of transistor TR4 rises and the voltage at output Y follows. Thus, output Y is HIGH if either or both of the inputs are HIGH, and the circuit acts as an OR logic function. As transistor TR4 turns OFF, either transistor TR2 or TR3 turns ON and their collector voltage falls. Output X also falls, giving a logic 0 output. This output produces a NOR logic function.

Q3 Two logic gates are connected as shown in Fig. 2.

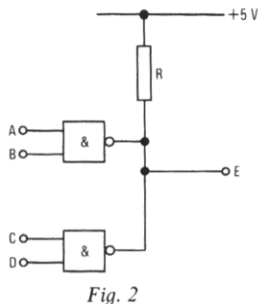
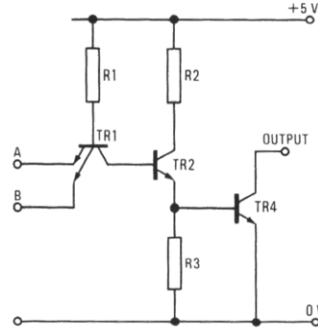


Fig. 2

- Name the type of output circuit required in each gate.
- Draw the circuit diagram for one of the gates.
- Draw the truth table for the circuit.

(5 min)

A3 (a) Each gate must have an open-collector output stage to allow them to be connected as shown. (b)



(c) The truth table for the circuit is as follows:

A	B	C	D	E
0	0	0	0	1
0	0	0	1	1
0	0	1	0	1
0	0	1	1	0
0	1	0	0	1
0	1	0	1	1
0	1	1	0	1
0	1	1	1	0
1	0	0	0	1
1	0	0	1	1
1	0	1	0	1
1	0	1	1	0
1	1	0	0	0
1	1	0	1	0
1	1	1	0	0
1	1	1	1	0

Q4 Identify the circuit shown in Fig. 3 and briefly describe its operation when clock pulses are applied. Assume that the outputs A, B, C and D are logic 0, 0, 0, and 0, respectively, and that its input is held at logic 1. (6 min)

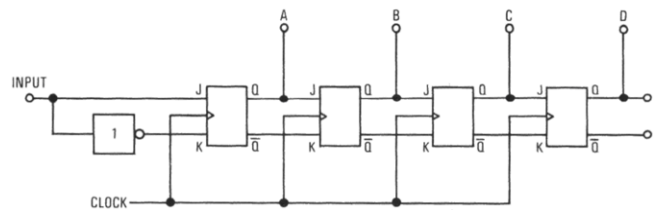


Fig. 3

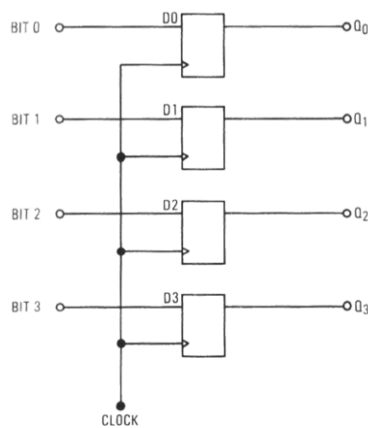
A4 The circuit shown in Fig. 3 is a 4 bit shift register.

If the input to the circuit is at logic 1, then the J and K inputs of the first bistable circuit are logic 1 and 0, respectively. This is the SET condition: when a clock pulse is applied, the output of bistable circuit A is set to logic 1. The inputs to the other stages of the shift register are derived from the previous stages. If the Q output is at logic 1, then the Q output must be logic 0. This is the RESET condition for the bistable circuit: when the clock pulses are applied, logic 0 is transferred to each Q output. The truth table for the first four clock pulses is as follows:

Clock Pulse	A	B	C	D
	0	0	0	0
1	1	0	0	0
2	1	1	0	0
3	1	1	1	0
4	1	1	1	1

Q5 Draw a diagram to show how four D-type bistable circuits can be connected to make a 4 bit register with parallel input and output connections. (3 min)

A5



Q6 Describe what is meant by the term 'universal shift register'. (2 min)

A6 A universal shift register is one which has facilities for both serial and parallel inputs. It also has serial and parallel outputs and is capable of shifting its data in either direction.

Q7 Compare commonly available transistor-transistor logic (TTL) and complementary metal-oxide semiconductor (CMOS) shift registers in terms of their speed of operation, power consumption and circuit complexity. (5 min)

A7 Speed of Operation

Generally, TTL circuits are faster than their CMOS equivalents, and this is true of shift registers. For example, the 74194 4-bit universal shift register can operate at clock rates of up to 25 MHz, whereas the 4035, a similar CMOS circuit, can be used at clock rates of up to only 10 MHz with a 5 V supply.

Power Consumption

CMOS circuits tend to dissipate much less power than their equivalent TTL circuits. For example, at 10 MHz, the power dissipation of a 4035 circuit is about 60 mW, whereas the dissipation of a 74194 circuit is 195 mW.

Circuit Complexity

Because of the greater packing density of CMOS chips, their circuits can be made more complex than TTL chips. For example, CMOS shift registers such as the 4557 circuit are available which can be programmed to have lengths of between 1 and 64 stages. The 4731 circuit contains four independent 64-stage shift registers.

Q8 Give three applications for an integrated-circuit shift register. (2 min)

A8 Typical applications include

- (a) serial arithmetic circuits such as adders or multipliers, where shift registers are used to hold the numbers;
- (b) serial-to-parallel and parallel-to-serial converters; and
- (c) digital delay circuits, which delay a pulse train by a length of time that is dependent upon the number of stages in the shift register and the clock rate.

Q9 The 7493 circuit is a typical transistor-transistor logic (TTL) binary counter. Use the pin connection diagram for the circuit given in Fig. 4 to show how it could be connected as a decade counter. Explain any connections required. (2 min)

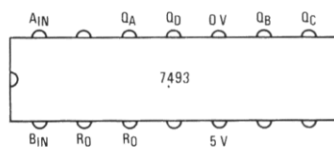
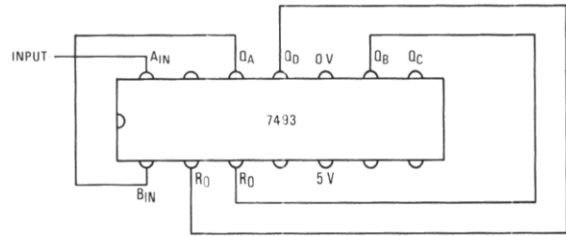


Fig. 4

A9 The 7493 circuits can be made to operate as a decade counter by connecting it as shown in the sketch.



The counter must be RESET to 0000 when the count 1010 appears at its outputs. Therefore, by connecting outputs B and D to the reset inputs R_0 , this function can be achieved. Since bistable circuit A is not connected to bistable circuits B, C and D internally in the 7490 circuit, this connection must also be made. Input pulses are then applied to input A_{IN} , pin 14. The output is taken from output Q_D .

Q10 Fig. 5 shows a simplified minutes-and-seconds timer controlled by a crystal. Answer the following questions.

- (a) What should the frequency of the crystal be?
- (b) What is the function of block A?
- (c) What is the function of block B?

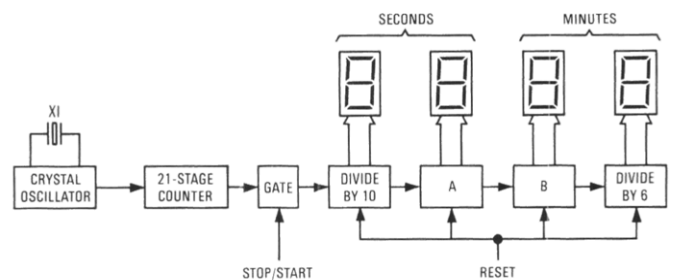


Fig. 5.

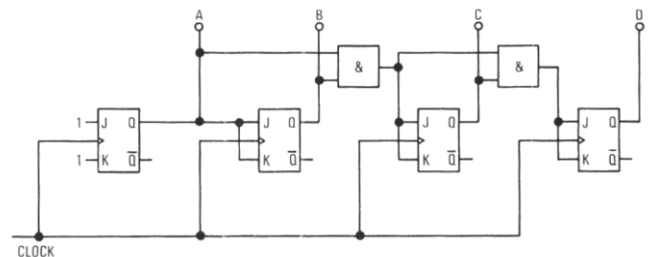
A10 (a) The divide-by-10 circuit counts the seconds and therefore requires an input of 1 pulse/s. The 21-stage counter divides the frequency of the crystal by 2^{21} . Thus the division ratio is 2097152. The crystal must therefore have a frequency of 2.097152 MHz.

(b) Block A counts the tens-of-seconds. Since these can be between 0 and 5, block A must be a divide-by-6 counter.

(c) Block B counts the minutes, which may be between 0 and 9. Block B must therefore be a divide-by-10 counter.

Q11 Draw the circuit diagram of a synchronous binary counter capable of counting from 0 to 15. (5 min)

A11 A synchronous binary counter is shown in the sketch.



Q12 For each of the statements given below, state whether they are true or false, and give your reason.

- (a) The speed of operation of an asynchronous binary counter is limited only by the maximum clock rate for the type of logic gate used in its construction.
- (b) Complementary metal-oxide semiconductor (CMOS) counters can operate at the same speed as transistor-transistor logic (TTL) counters for the same supply voltage.
- (c) Master-slave bistable circuits help to avoid the occurrence of dynamic hazards in synchronous counters.
- (d) Asynchronous counters generate spurious output states of very short duration between their true counts. (8 min)

A12 (a) False. Asynchronous counters suffer from ripple-through delay, which limits their maximum operating speed.

(b) False. Generally, CMOS counters can operate only at clock rates of up to about 5 MHz, whereas TTL counters operate at up to 25 MHz, for a 5 V supply.

(c) True. Since the outputs of master-slave bistable circuits cannot change while their inputs are changing, dynamic hazards can be avoided.

(d) True. The ripple-through delay in asynchronous counters means that bistable circuits at the 'most significant' end of the counter change state a short time after those earlier in the chain. This delay leads to momentary false counts being present on the outputs.

Q13 With the aid of a count sequence table, explain the operation of the counter shown in Fig. 6. (6 min)

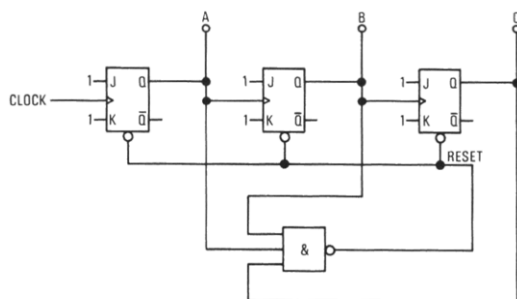


Fig. 6

A13 The circuit shown in Fig. 6 is a divide-by-7 asynchronous counter. The sequence table for the circuit is as follows:

Clock Pulse	C	B	A
0	0	0	0
1	0	0	1
2	0	1	0
3	0	1	1
4	1	0	0
5	1	0	1
6	1	1	0
7	0	0	0

The sequence then repeats from clock pulse 1

If the counter starts off at 000, then the output of the NAND gate is HIGH and the circuit is not reset. The count proceeds in the standard binary sequence as clock pulses are applied.

On the arrival of clock pulse 7, the counter outputs momentarily go to 111. This generates logic 0 at the output of the NAND gate, which then resets all the bistable circuits to logic 0. Therefore, the count appears to go directly from 110 to 000; this gives a 7-stage count.

Each counter stage is a J-K bistable circuit connected so that it operates as a toggle. On the negative-going edge of the clock pulse, each bistable circuit changes state, although there is a small ripple-through delay because of the asynchronous configuration.

Q14 Sketch the waveforms of outputs A, B and C and the clock input of the counter shown in Fig. 7. Assume that outputs A, B and C are initially at 000. Indicate the binary number present on the outputs shown for each clock pulse. (6 min)

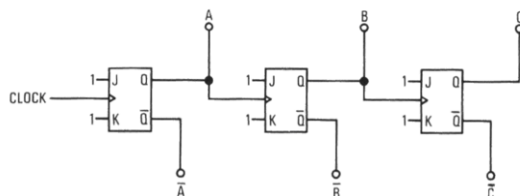
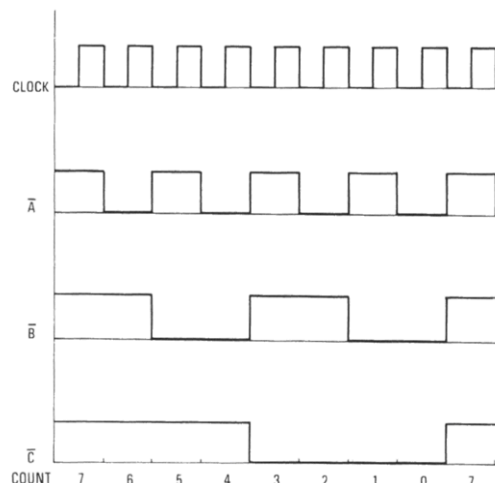


Fig. 7

A14 The waveforms at A, B and C are shown in the sketch.



Q15 A J-K bistable circuit is to be used as a divide-by-2 element in a counter. Which of the following connections to the J and K inputs should be made?

- (a) J to logic 1, and K to logic 0.
- (b) J to logic 0, and K to logic 1.
- (c) Both J and K to logic 1.
- (d) Both J and K to logic 0.

(1 min)

A15 (c) Both J and K to logic 1.

Q16 Fig. 8 shows a switch debouncing circuit. Briefly explain its operation; assume that transistor-transistor logic (TTL) gates are used. (6 min)

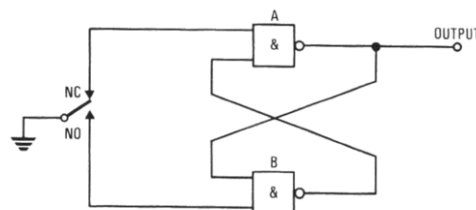


Fig. 8

A16 The switch in the circuit is normally in the position shown. This puts logic 0 onto one of the inputs of gate A, and the output is held at logic 1. The open-circuit connection to the input of gate B appears as logic 1 and therefore the output of gate B is at logic 0.

When the switch is moved, it first leaves the NC (normally closed) connection, which rises to logic 1. Any bounce at this contact does not affect the output state, which remains at logic 1. As soon as the switch wiper reaches the NO (normally open) connection, it places logic 0 on one of the inputs to gate B, and this therefore changes state. As the output of gate B rises to logic 1, it forces the output of gate A to logic 0. If the wiper bounces on this contact, the output of gate B cannot change and so the output remains at logic 0.

When the switch is returned to its NC connection, the reverse of the above occurs. At no time can any contact bounce affect the output, which is therefore a clean negative-going pulse as the switch is closed and then opened again.

Q17 Choose one of the answers given below to complete the following sentence:

A master-slave bistable circuit is preferred to a non-master-slave bistable circuit because

- (a) it operates at higher speed.
- (b) its outputs cannot change if the inputs change when the clock pulse is at logic 1.
- (c) it does not exhibit a ripple-through delay.
- (d) it has no indeterminate state.

(1 min)

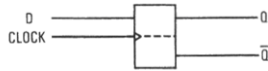
A17 (b) its outputs cannot change if the inputs change when the clock pulse is at logic 1.

Q18 Draw the circuit symbol for the type of bistable circuit that has a truth table as follows:

Clock	Input	Q	$\bar{Q}$
0	0	Previous Q	Previous $\bar{Q}$
1	0	0	1
0	1	Previous Q	Previous $\bar{Q}$
1	1	1	0

(2 min)

A18 The circuit is for a D-type bistable circuit; the circuit symbol is shown in the sketch.



Q19 Complete the truth table given below for a gated S-R bistable circuit constructed from four NAND gates.

Clock	S	R	Q	$\bar{Q}$	Comment
0	X	X			
1	0	0			
1	0	1			
1	1	0			
1	1	1			

(4 min)

A19

Clock	S	R	Q	$\bar{Q}$	Comment
0	X	X	Previous Q	Previous $\bar{Q}$	Memory state
1	0	0	Previous Q	Previous $\bar{Q}$	Memory state
1	0	1	0	1	RESET state
1	1	0	1	0	SET state
1	1	1	1	1	Indeterminate

Q20 The circuit given in Fig.9 shows a simple S-R bistable circuit. Derive its truth table and hence comment on the states which it can adopt. (4 min)

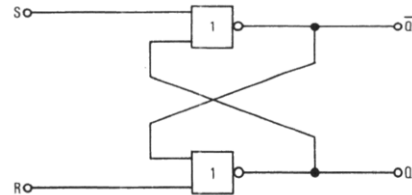


Fig. 9

A20 The truth table for the NOR-gate version of an S-R bistable circuit is as follows:

S	R	Q	$\bar{Q}$	Comment
0	0	Previous Q	Previous $\bar{Q}$	Memory state
0	1	0	1	RESET state
1	0	1	0	SET state
1	1	0	0	Indeterminate

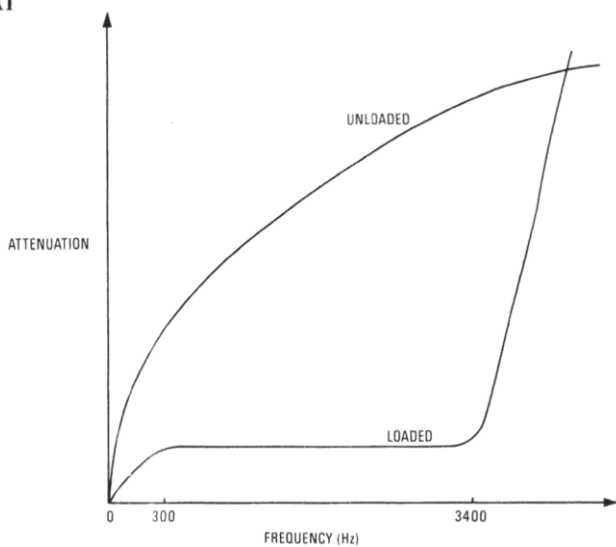
Questions and answers contributed by D. Turner

BTEC: TRANSMISSION SYSTEMS III

The questions in this paper are based on BTEC's standard unit U81/741. Students are advised to read the notes on p. 29

Q1 Draw and label a graph to show the effects, on the commercial speech range, of loading an audio cable. (4 min)

A1



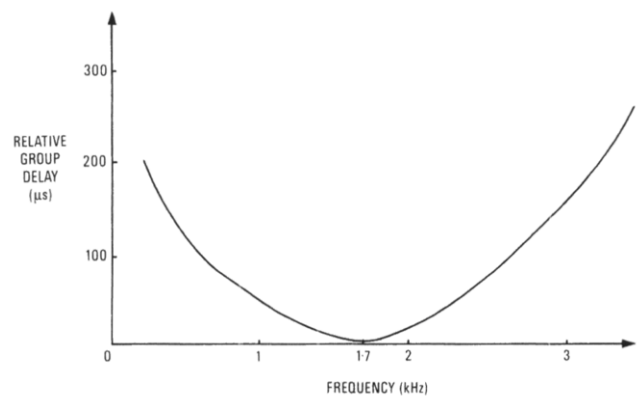
[Tutorial note: For an unloaded cable, there is about 1.5 dB/km spread over the commercial range.]

Q2 What are the two main losses incurred by signals transmitted over a cable? (2 min)

- A2** (a) Power reduction, varying with frequency, expressed in decibels, and
(b) propagation delay, varying with frequency, expressed in units of time.

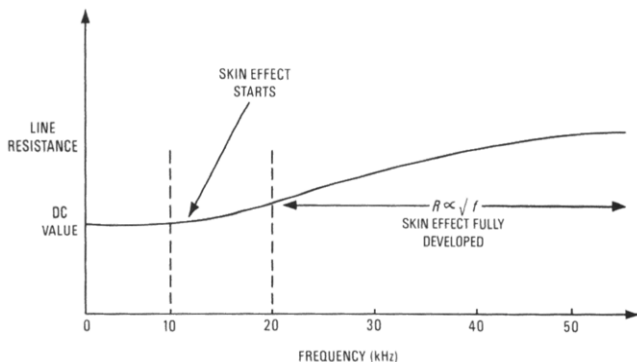
Q3 Draw a graph to show the relative group-delay/frequency curve of a telephony carrier channel. (4 min)

A3



Q4 Explain, with the aid of a graph, the way in which the resistance of a transmission line conductor varies with frequency. (6 min)

A4 At very-low frequency, the resistance is constant and equal to the DC value but, as the frequency is increased further, the skin effect becomes apparent and the resistance begins to increase. When the skin effect is fully developed, the resistance becomes proportional to the square root of the frequency. This is illustrated in the sketch.



Q5 (a) State the minimum attenuation/frequency distortion equation for a transmission cable and give its units.
(b) Explain briefly what is meant by

- (i) continuous loading, and
- (ii) lumped loading.

(4 min)

A5 (a) Minimum attenuation/frequency distortion exists when

$$LG = RC$$

where L is the inductance in henrys, G is the conductance in siemens, R is the resistance in ohms and C is the capacitance in farads.

(b) (i) In continuous loading, the transmission line conductors are wrapped continuously along their length with wires of a high-permeability ferromagnetic material.

(ii) In lumped loading, inductors are inserted into the cable at regular intervals.

Q6 State whether the following expressions of group-delay times (T_g), for various frequency ranges, on audio unloaded and coaxial cables are true or false.

- (a) At a frequency below a few hundred hertz, $T_g \approx \sqrt{(RC)}$.
- (b) At a frequency up to 3 kHz, $T_g \approx \sqrt{(3RC/8\omega)}$
- (c) At a frequency above 30 kHz, $T_g \approx \sqrt{(LC/\omega)}$

R is the loop resistance in ohms/kilometre loop, C is the capacitance in farad/kilometre, L is the inductance in henrys/kilometre loop and $\omega = 2\pi \times \text{frequency}$. (5 min)

A6 (a) True

- (b) False [Tutorial note: $T_g \approx \sqrt{(RC/8\omega)}$]
- (c) False [Tutorial note: $T_g \approx \sqrt{(LC)}$]

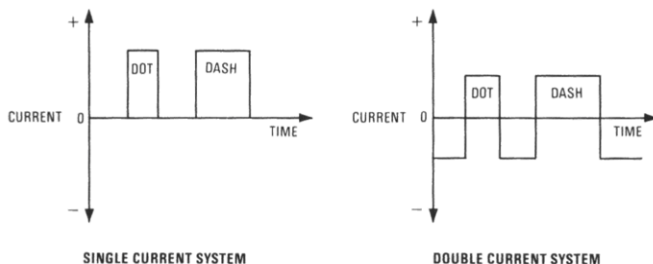
[Tutorial note: Between 3 kHz and 30 kHz there is no approximate expression for group delay time.]

Q7 In DC telegraph working, two systems of signalling are used. State

- (a) both systems used, and
- (b) draw a diagram to show a dot followed by a dash (morse code letter 'A') for both systems. (6 min)

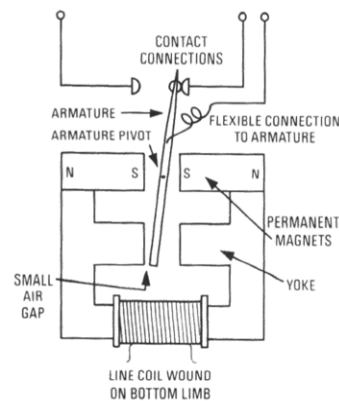
A7 (a) The two systems are single current and double current.

(b)



Q8 Draw and label a diagram of a polarised relay (Carpenter type) and give a brief explanation of how it works. (10 min)

A8



The Carpenter-type polarised relay produces very little distortion because of its special construction. It has a very finely balanced armature, which is itself a moving contact. There are two fixed contacts. When current is flowing in one direction the armature contact is made with one of the fixed contacts; when the current in the relay changes direction, the armature changes over very quickly to the other fixed contact. Hence, there are no operate and release positions as there are in an ordinary relay; either contact can be designated the 'normal' or as the 'operate' position. It is very sensitive and can operate at very high speed.

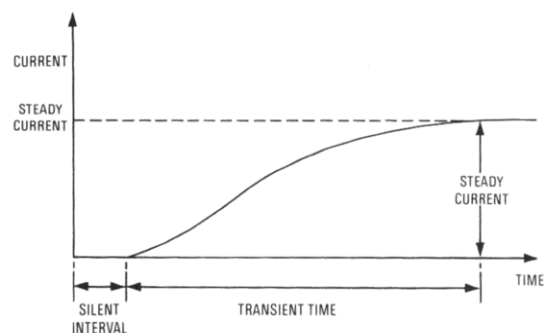
Q9 Explain briefly the advantage of the double-current system over the single-current system. (6 min)

A9 The reversals of polarity in double-current systems assist the discharge of line capacitance, thus increasing the initial rate of growth and decay current, and therefore making it possible to achieve higher signalling speeds. The receiving relay in a double-current system is more reliable in operation because

- (a) continual reversals prevent the build-up of residual magnetism,
- (b) the marking and spacing currents being continuously present minimise leakage currents and inductive disturbances, and
- (c) the relay does not require bias adjustment to take account of longer lines or changes in line parameters.

Q10 Sketch a typical arrival curve for a long unloaded cable. (4 min)

A10



Q11 State three advantages of voice-frequency signalling over DC signalling. (5 min)

- A11** (a) Voice-frequency (VF) signals can be amplified by using standard telephony amplifiers.
- (b) There is no limit to the distance over which a VF signal can be transmitted.
- (c) The same line plant can be used for signalling and telephony circuits, thereby avoiding the need to provide separate signalling cables and enabling the telephony and transmission systems to be completely integrated.

Q12 Explain the term 'bit rate' and calculate the bit rate in bit/s if the duration of 1 bit is 1.666 ms. (5 min)

A12 Bit rate is the speed at which the data is sent and is expressed in bits per second. A bit is one binary digit, a '1' or '0'.

The bit rate is given by $1/t$, where t is the duration of one bit in seconds. Thus, for the example given, the bit rate is $1/1.666 \times 10^{-3} = 600 \text{ bit/s}$.

Q13 Which of the following frequencies is the one used as a carrier frequency for phase modulation on the British Telecom system?

- (a) 1000 Hz, (b) 1300 Hz, (c) 1800 Hz or (d) 2100 Hz. (2 min)

A13 (c) 1800 Hz [Tutorial Note: A carrier frequency for a phase-modulation system is normally chosen midway in the telephony band.]

Q14 A data link is set up using a speed of 600 bit/s and carrier frequency of 1200 Hz and 1800 Hz. Determine the bandwidth required for the link. (4 min)

A14 If R is the bit rate, F_1 is the highest carrier frequency and F_2 is the lowest carrier frequency, then

$$\begin{aligned} \text{bandwidth} &= 2R + F_1 - F_2 \\ &= 2 \times 600 + 1800 - 1200, \\ &= 1200 + 600, \\ &= 1800 \text{ Hz.} \end{aligned}$$

Q15 State the three basic principles for the generation of a digital signal on a pulse-code modulation (PCM) system. (2 min)

- A15** (a) Pulse-amplitude modulation
(b) Quantizing
(c) Encoding

Q16 Which quantum level describes a single sample whose amplitude is 0.451 V, given that each quantum level represents a step of 0.01 V? (2 min)

A16 Quantum level number 45.

Q17 How many binary digits are required to represent 512 quantum levels? (2 min)

A17 Nine binary digits.

Q18 Calculate the percentage reduction in quantizing error when the number of quantum levels is

- (a) increased from 16 to 128, and
(b) increased from 16 to 256. (4 min)

A18 (a) The increase in the number of levels is 8 times. Therefore, the error is reduced by 0.125 or by 87.5%.

(b) The increase in the number of levels is 16 times. Therefore, the error is reduced by 0.0625 or by 93.75%.

[Tutorial note: The amplitude of the quantization noise depends on the size of the quantization steps and can be reduced by reducing the size of the steps; that is, increasing the number of quantum levels.]

Q19 Complete the following statements.

(a) A 30 channel pulse-code modulation (PCM) system has a time-slot per channel of

(b) The system has 32 time-slots in total, ... (i) are dedicated to carrying telephony and ... (ii) are used for signalling and synchronisation.

(c) Each time slot contains a bit word.

(d) The first digit in each time-slot describes the ... (i) of the sampled signal, the remaining digits describe the ... (ii) ... (5 min)

A19 (a) 3.9 μs .

- (b) (i) 30 (ii) 2
(c) 8
(d) (i) polarity (ii) amplitude

Q20 Calculate the bit rate of a pulse-code modulation (PCM) system that has a sampling rate of 8 kHz, 30 channels and 256 binary codes. (5 min)

A20 Bit rate = sampling frequency $\times$ number of channels $\times$ number of binary digits in the code,

$$\begin{aligned} &= 8 \times 10^3 \times 8 \times 30, \\ &= 1.92 \text{ Mbit/s.} \end{aligned}$$

Q21 Which of the following produces white, sometimes known as thermal, noise?

- (a) A relay contact
(b) Teleprinters
(c) A spark
(d) An amplified circuit (2 min)

A21 (d) An amplified circuit

Q22 A ray of light passes through a glass block of refractive index 1.7. Calculate the angle of incidence that produces total internal reflection of the ray of light back into the glass block. (5 min)

A22

$$\mu = \frac{\sin i}{\sin r} \text{ for air to glass.}$$

$$\mu = \frac{\sin r}{\sin i} \text{ for glass to air.}$$

$$\therefore 1.7 = \frac{\sin 90^\circ}{\sin i},$$

$$= \frac{1}{\sin i}.$$

$$\therefore \sin i = \frac{1}{1.7},$$

$$= 0.5882.$$

$$\therefore i = \sin^{-1} 0.5882,$$

$$= 36^\circ 2'.$$

Where μ = the refractive index, i = angle of incidence, and r = angle of refraction.

Q23 State the two transmission modes used in optical-fibre communications. (2 min)

A23 (a) Multimode
(b) Single-mode [Tutorial Note: Single-mode was previously known as monomode.]

Q24 Which of the following bandwidths would be the highest a system using a laser and single-mode fibre would be able to accommodate?

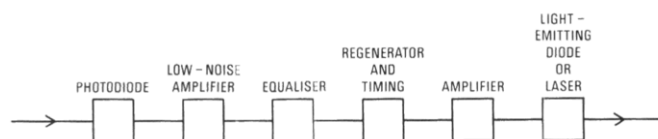
- (a) 5 MHz (b) 10 MHz (c) 20 MHz
(d) 100 MHz (e) 1000 MHz (3 min)

A24 (e) 1000 MHz

[Tutorial Note: The designed practical bandwidth of an optical-fibre system can vary quite significantly depending on the components used to construct the system; for example, a near infinite bandwidth system of over 1 GHz using a laser connected to a single-mode fibre.]

Q25 Draw a block diagram of an intermediate regenerator that could be used on an optical-fibre system. (4 min)

A25



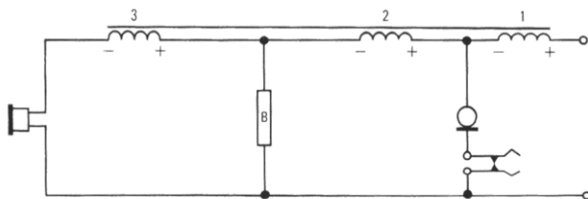
Questions and answers contributed by P. Ritchie

BTEC: TELECOMMUNICATIONS SWITCHING SYSTEMS II

The questions in this paper are based on the BTEC's standard unit U81/753. Students are advised to read the notes on p. 29

Q1 Explain, with the aid of a simplified circuit diagram of the elements of a modern telephone instrument, how incoming speech currents operate a rocking armature receiver. (10 min)

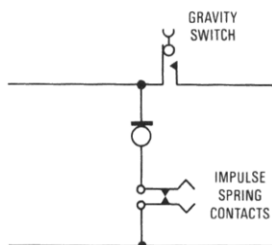
A1 The relevant elements of a telephone-instrument circuit are shown in the sketch.



The incoming speech current flows speech mainly via coil 1, the microphone and the impulse springs. Coil 1 acts as a primary winding of a transformer and induces EMFs in the other coils as indicated. The EMF generated in coil 3 causes speech currents to flow via the receiver. The circuit arrangements are such as to prevent current flowing in the balance circuit, B, and, therefore, zero power is dissipated in the balance circuit.

Q2 With the aid of a simple circuit diagram of the relevant parts of a telephone instrument, explain how the calling signal is originated to the exchange and hence how the necessary routing information is transmitted on the receipt of dial tone. (10 min)

A2 The relevant components of a telephone instrument are shown in the sketch.

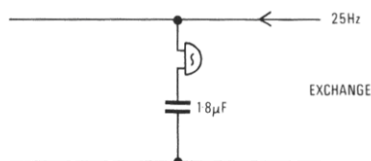


The lifting of the handset causes the gravity-switch contact to operate, completing the calling loop to the telephone exchange. If a first selector is free, dial tone is returned to the caller. The caller then operates the dial which, on its return movement operates the dial impulse spring contacts, breaking the loop the appropriate number of times with a ratio of 2 : 1 break to make and a speed of 10 pulses/s.

Q3 State the form of signalling used to operate a telephone bell and show, with a simple circuit diagram, how the bell is connected in the instrument. (5 min)

A3 The bell is operated by an alternating current of 25 Hz which is interrupted to give the required cadence.

The appropriate part of the telephone circuit is shown in the sketch. The bell is connected in series with a $1.8 \mu\text{F}$ capacitor and is effectively connected across the local-line pair. The capacitor prevents a permanent DC calling loop being applied across the line.



Q4 (a) List the disadvantages of excessive sidetone that occur when the caller is speaking.

(b) Explain whether excessive sidetone on the receiving telephone would cause any problems and, if so, state what they are. (8 min)

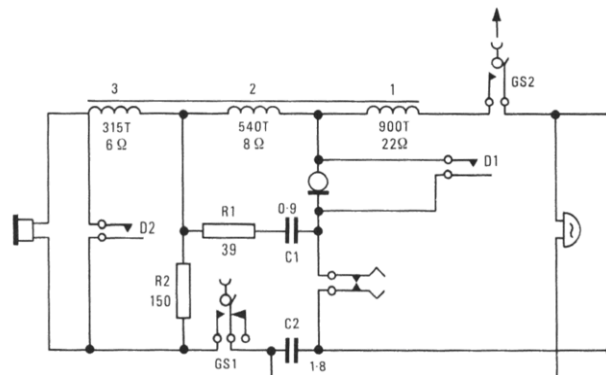
A4 (a) Excessive sidetone would

- (i) waste power,
- (ii) cause the speaker to lower his voice, and
- (iii) cause ear fatigue.

(b) If excessive sidetone existed at the listening end, hearing would be difficult, especially in a noisy environment, because room noise would be heard in the receiver.

Q5 Draw the circuit elements of a telephone instrument and list the functions of each component. (20 min)

A5



The microphone converts acoustical energy to electrical energy. The receiver converts electrical energy to acoustical energy. Contacts GS1 and GS2 connect the telephone to the line when the handset is lifted and disconnect it when the handset is replaced.

Contacts D1 and D2 are dial-off-normal contacts which operate when the dial is turned from its normal position. They short circuit the microphone and receiver during dialling.

Capacitor C2 is effectively in series with the bell and prevents a permanent DC loop being presented to the telephone exchange.

Capacitor C1, together with resistors R1 and R2, form a spark-quench circuit; they also form the balance network across the induction coil.

Induction coils 1, 2 and 3 form an auto-transformer which divides the incoming and outgoing speech currents between the receiver and the line.

Q6 Explain how the calling customer's calling signal is recognised by a TXE2 telephone exchange, and what action results from such a signal. (5 min)

A6 When the caller lifts the handset, a loop is established which operates relay LR in the subscriber's line circuit at the telephone exchange. The operation of this relay causes the discharge of a capacitor through the calling-number generator which generates the caller's number in a 2-out-of-5 code. This is passed to, and stored in, the register.

Q7 Explain how the calling customer's signal is recognised by a TXE4 telephone exchange. State how many crosspoints need to be operated in order to return dial tone to the caller. (5 min)

A7 Each line termination on a TXE4 telephone exchange is continuously scanned by the scanning device. In the case of a calling-line termination, this scan is every 150 ms. Once a calling signal has been recognised, the main control unit causes a connection to be set up between the caller and a free register, from which dial tone is returned to the subscriber.

A total of seven matrix crosspoint switches needs to be operated.

Q8 In an established own-exchange call on a TXK1 telephone exchange, state what device will recognise a caller's clear-down condition and what action it needs to take. (5 min)

A8 After the common-control equipment had released, the line transmission relay group (LTRG) controls all call supervision and thus will note the caller has cleared. This will then remove the holding condition from all crosspoints, allowing them to release and clear the connection.

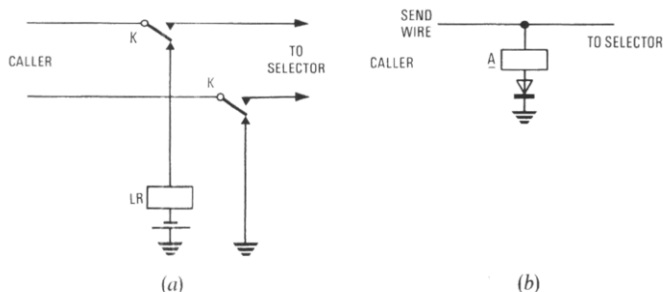
Q9 (a) Explain the difference between the calling of

- a telephone exchange, and
- a Telex exchange.

(b) With simple circuit diagrams show how the exchange receiving line relay is connected in each case. (10 min)

A9 (a) A telephone customer signals to the exchange by presenting a loop to the line. This causes relay LR to operate at the telephone exchange. (See sketch (a)).

(b) Although the Telex system uses the local-line network, one wire is used for sending and the other for receiving. To call the exchange, the caller operates a CALL key which connects a MARK condition (-80 V). The resulting change of potential causes the operation of relay A at the Telex exchange. (See sketch (b)).



Q10 For a Telex call, list the sequence of events which occur on the origination and establishment of a call. (8 min)

A10 (a) When the CALL key is operated a MARK condition (-80 V) is connected to the send line.

(b) The Telex exchange receive relay operates, extends the call to a selector and returns the *proceed-to-send* signal ($+80\text{ V}$) on the receive line.

(c) On recognition of the signal, the calling station dims the CALL lamp and starts the machine.

(d) The caller dials (-80 V and $+80\text{ V}$ pulses).

(e) The Telex exchange routes the call to the wanted number and signals to the receiving station with -80 V on the send line to start the motor of the receiving machine. When the motor has attained the correct speed, the *answer-back* signal is automatically sent to the caller.

Q11 What action is necessary at a Telex customer's station in order to clear down a connection? What conditions result in order to release both line and exchange equipment? (7 min)

A11 CLEAR keys are provided on the Telex signalling equipment, the operation of which connects $+80\text{ V}$ to the respective SEND wires. This causes the exchange controlling relay to release, which in turn releases each line and Telex machine.

Q12 State the type of telephone exchanges which use reed-relay matrices and respectively replace

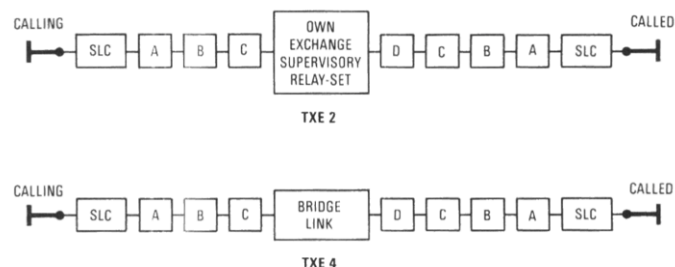
- small non-director telephone exchanges, and
- director telephone exchanges.

Draw a trunking diagram to show the routing of an established own-exchange call on ONE of the above exchanges. (10 min)

A12 (a) TXE2
(b) TXE4

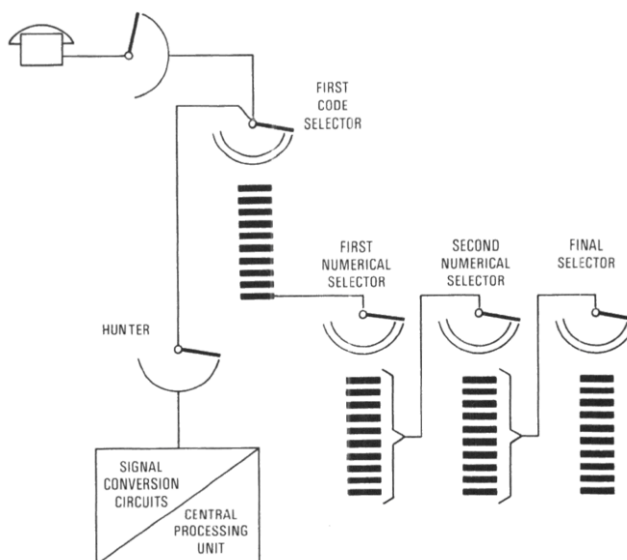
One of the following diagrams was required.

'A', 'B' etc. refer to switching stages



Q13 Draw a trunking diagram to show the routing of an own-exchange call through a director telephone exchange that uses stored-programme-control (SPC) equipment. State two advantages of SPC over electro-mechanical equipment. (10 min)

A13



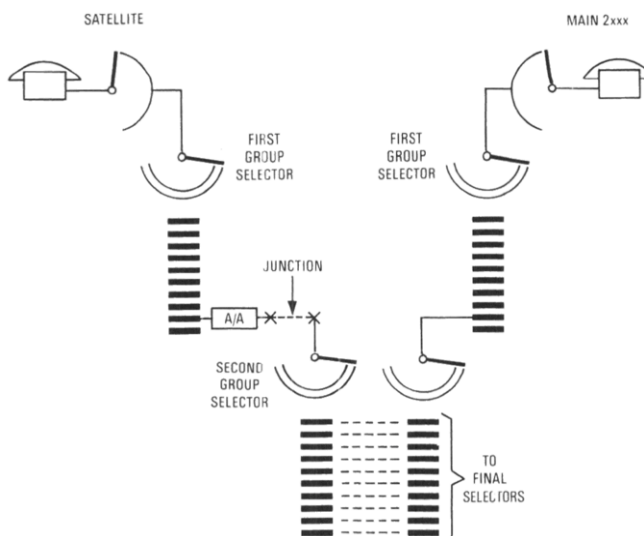
The advantages of SPC equipment over electromechanical equipment are:

- it is quicker in operation,
- it requires less floor space,
- it is quieter in operation, and
- consumes less power.

Q14 Draw a trunking diagram to show the routing of a call from a customer on a satellite telephone exchange to a customer on the main telephone exchange in a non-director multi-exchange area. State the main advantages of such an area. (10 min)

A14

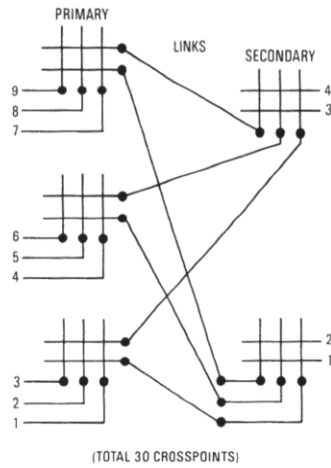
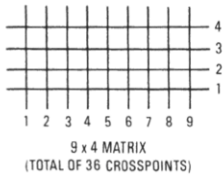
The main advantage of a multi-exchange area is the saving of line plant.



Q15 Show, with the aid of a diagram, how the nine inlets of a matrix switch can be connected to any of 4 outlets.

With a second diagram, show how a two-stage trunking scheme can connect the same number of inlets to the same number of outlets, but using less crosspoints. (10 min)

A15



Q16 (a) The two-stage trunking diagram shown in Fig. 1 could cause calls to be lost because of link blocking. Explain this by way of an example.

(b) Draw a trunking diagram and describe a tertiary switching stage which would reduce link blocking. (15 min)

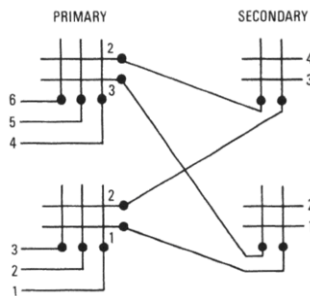
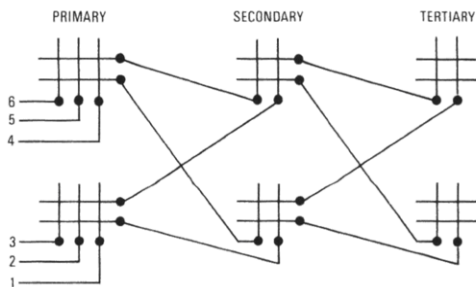


Fig. 1

A16 (a) If inlet 1 is connected to outlet 1 via crosspoint 1,1, then inlet 2 or inlet 3 to outlet 2 would be blocked.

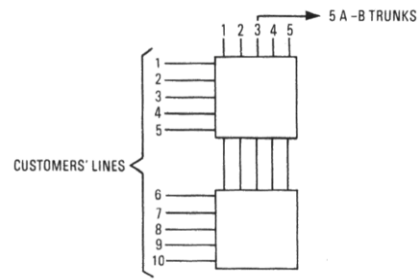
(b)



In the three-stage matrix shown in the sketch, it can be seen that inlet 2 or inlet 3 could be connected to outlet 2 by a different secondary switch.

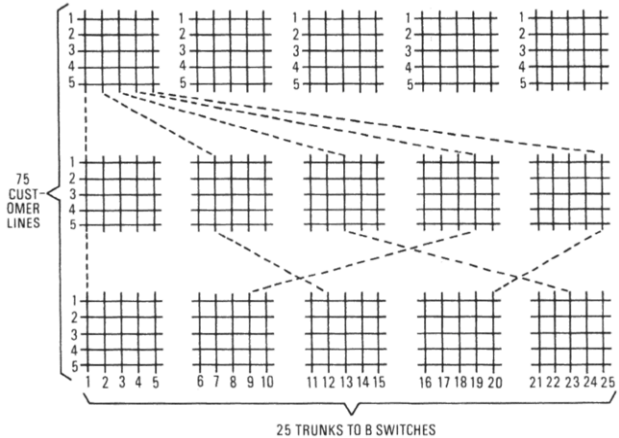
Q17 On a simple sketch, show how 10 customers' lines are connected to two A switches, so that they all share the same five A-B trunks. (5 min)

A17



Q18 With the aid of a sketch, explain the principle of the slipped multiple as used on a typical A switch. (15 min)

A18



The sketch shows a 75-line switch made up of fifteen 5×5 units. A normal multiple connection would show the vertical connections made as 1 to 1, 2 to 2, 3 to 3, etc. Such an arrangement leads to congestions since 5 simultaneous calls out of a group of 25 would block access to the B switches.

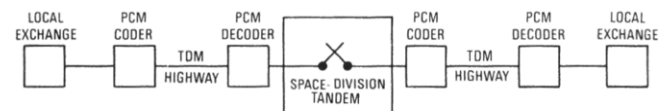
To minimise this risk within the switch group, the five rows are interconnected as a slipped multiple. The first trunk only is connected through the above rows; the second trunk is slipped one to the right as it moves through the three rows; the third trunk is slipped two to the right; and so on.

Thus, if any one group of the five A-to-B trunks is busy, the B switch will be accessible via one of the other groups.

Q19 (a) Draw a block diagram to show the routing of a pulse-code modulation (PCM) system via a conventional space-switched tandem telephone exchange.

(b) Explain what savings are made when time-space-time (TST) switches are used in a tandem telephone exchange. (10 min)

A19 (a)



As can be seen from the sketch, it is necessary to decode the PCM system into audio channels before switching can take place and then to encode the traffic again for transmission over the time-division multiplex highway.

(b) In a tandem telephone exchange with TST switches, the channels are digitally switched, which renders the decoding and re-encoding equipment unnecessary.

Questions and answers contributed by N. A. Collins

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